REMARKS

In an Office Action mailed on December 3, 2002, objections were made to claims 3 and 24; claims 1-6, 8-14 and 16-21 were rejected under 35 U.S.C. § 102(e) as being anticipated by Melo; claims 7 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Melo in view of alleged admitted prior art; and claims 22-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Melo. Claims 3 and 24 have amended to overcome the objections to these claims. The §§ 102 and 103 rejections of the claims are addressed below.

A marked-up version of the amended claims is submitted as a separate document. The undersigned has endeavored to ensure that the clean and marked-up versions of the amended claims correspond. However, the Examiner is specifically requested to verify that these two versions of the claims are consistent.

Rejections of Claims 1-10:

The computer system of claim 1 includes a local bus, a memory bus and a buffer. The memory bus is capable of indicating data. The buffer is adapted to capture the data directly from the memory bus, and the buffer is located closer to the local bus than to the memory bus.

In contrast, Melo discloses a buffer 306 that is shown in Fig. 3 as being coupled to the bus 103 and the memory controller 210. In the corresponding text, Melo describes the buffer 306 as being part of a feedback path for data that is read from main memory 104. Melo, 8:1-2. However, Melo does not teach or even suggest that the buffer 306 captures data directly from the memory bus 106. Instead, Fig. 3 clearly depicts the buffer 306 as being connected to the memory controller 210, and in Fig. 2, Melo shows the memory controller 210 as being connected to the main memory 104. Thus, it is the memory controller 210 that captures data directly from the memory bus 106, not the buffer 306. Therefore, Melo fails to teach or even suggest a buffer that is adapted to capture data directly from a memory bus and is located closer to the local bus than to the memory bus.

Therefore, for at least this reason, withdrawal of the § 102 rejection of claim 1 is requested. Claims 2-10 are patentable for at least the reason that these claims depend from an allowable claim.

Rejections of Claims 11-17:

The bridge of claim 1 includes a local bus interface that is located closer to a local bus than to a memory bus. This local bus interface includes a buffer that is adapted to capture indications of data from the conductive traces near a second region near the local bus to directly capture data from the memory bus.

The Examiner contends the buffer 306 of Melo constitutes the buffer of the bridge of claim 11. However, as discussed above in connection with claim 1, Melo neither teaches nor suggests that the buffer 306 captures data directly from the memory bus 106. Instead, the memory controller 210 of Melo captures data directly from the memory bus 106. Thus, Melo fails to teach all of the limitations of claim 11, and therefore, withdrawal of the § 102 rejection of claim 11 is requested. Claims 12-17 are patentable for at least the reason that these claims depend from an allowable claim.

Rejections of Claims 18-21:

The method of claim 18 includes capturing data directly from a memory bus in a buffer that is located closer to a local bus than to the memory bus.

For the reasons set forth below, Melo fails to teach capturing data directly from a memory bus in a buffer that is located closer to a local bus than to a memory bus. Therefore, withdrawal of the § 102 rejection of claim 18 is requested. Claims 19-21 are patentable for at least the reason that these claims depend from an allowable claim.

Rejections of Claims 22-26:

The method of claim 22 includes substantially extending a memory bus into a bridge. The memory bus is adapted to indicate data in a memory read operation. The method also includes capturing the data directly from the extension of the memory bus into the bridge.

Contrary to the limitations of claim 23, Melo fails to teach or suggest extending a memory bus into a bridge. The Examiner states "it would have been obvious to one skilled artisan at the time the invention was made to do in order to exchange data from the memory bus to a local bus faster." Office Action, p. 4. However, the Examiner fails to establish a *prima facie* case of obviousness. In this manner, to establish a *prima facie* case of obviousness, there must be a suggestion or motivation to modify the reference to obtain the missing claim limitations. Furthermore, the Examiner must specifically point out language in a prior art reference to support the alleged suggestion or motivation. *Ex parte Gambogi*, 62 USPQ2d 1209, 1212 (Bd. Pat. App. & Int. 2001); M.P.E.P. § 2143. Because the Examiner has failed to provide such support, a *prima facie* case of obviousness has not been established for claim 22. Claims 23-26 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, withdrawal of the § 103(a) rejections of claims 22-26 is requested.

CONCLUSION

In view of the foregoing, withdrawal of the §§ 102 and 103 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (MCT.0078US).

Respectfully submitted,

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CLAIM AMENDMENTS

The claims have been amended as follows:

3. (Amended) The computer system of claim 1, further comprising:

conductive traces adapted to communicate indications of the data from a first region near the memory bus to a second region near the buffer, the conductive traces [lines] introducing an approximate first asynchronous propagation delay in the communication.

24. (Amended) The method of claim 22, further comprising:

using conductive traces adapted to communicate indications of the data from a first region near the memory bus to a second region near the buffer, the conductive traces [lines] introducing an approximate first asynchronous propagation delay in the communication.